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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,157	06/27/2003	Hai Jiang		7873

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Fremont, CA 94539

EXAMINER
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LUU, PHO M

ART UNIT	PAPER NUMBER
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2824

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/609,157

Applicant(s)

JIANG, HAI

Examiner

Pho M. Luu

Art Unit

2824



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 28-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 28-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 09/23/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: Search History.

## **DETAILED ACTION**

### ***Reply to Election/Restrictions***

1. Applicant's election without traverse of Group II, Claims 28-31 filed 14 May 2005 is acknowledged. The changes and remarks disclosed therein were considered.
2. Claims 1-27 have been canceled.
3. Claims 28-31 are pending in the application.

### ***Information Disclosure Statement***

4. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 23 September 2003. The information disclosed therein was considered.

### ***Drawings***

5. The drawings were received on 27 June 2003. These drawings are review and accepted by examiner.

### ***Specification***

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: **"The Phase Change Resistive and Programming Metallization in Memory"**.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki et al. (US. 6,084,796) in view of Gonzalez et al. (US. 6,391,688).

For the purpose of this rejection, the resistive element such as a chalcogenide phase change memory as described in the specification in paragraph 019, lines 2-3 and the memory element including a ultra small resistive layer as described in the specification in paragraph 023, lines 6-7.

With respected to independent claim 28, Kozicki et al in Figure 1A-1B and Figure 5C discloses a programming metallization cell memory (10) comprising:

a pair of electrodes (13, 14 in Figure 1A-1B and 253, 254, 260, 262 in Figure 5C);

a thin metal layer (metal 15, example, when the metal 15 which is apply the voltage for removed the electrodes 13 and 14, see column 6, lines 5-9);

a single resistive layer (resistive 270, for example, 270 is a resistive material layer as shown in Figure 5C, see column 8, lines 50-58) with a plurality of solid electrolyte (ion conductor 12 in Figure 1A-1B including a solid electrolyte, see column 5, line 18-19).

However, Kozicki et al does not teach an ultra-small resistive element (as explain above, the resistive element such as chalcogenide memory).

Gonzalez et al in Figure 15 disclosed the ultra-small pore is the fabrication utilized of the chalcogenide memory cell (see column 6, lines 66-67 and column 7, lines 1-5).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify Kozicki et al by using an ultra-small resistive element such as chalcogenide memory cell with minimum dimensions and reducing the required energy input to the chalcogenide in the programming metallic cell as taught by Gonzalez et al.

With respected to dependent claim 29, Kozicki et al. in Figure 1B disclosed the top and bottom surface (electrode 13 and electrode 14 disposed at the surface of ion conductor including the electrolyte resistive element (12)) which is contact direct with the adjacent metal layer (15) and bottom electrode (electrode 13 such as cathode is negative electrode and electrode 14 such as anode is positive electrode, see column 5, lines 10-11).

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With respected to dependent claim 30, Kozicki et al. in Figure 1A-1B disclosed top and bottom surface (electrode 13 and electrode 14 disposed at the surface of ion conductor including the electrolyte resistive element (12)) which is contact direct with the adjacent of conductor layer (conductor layer such as electrically conducting will produce an electric field in electrode 13, electrode 14 and ion conductor including the electrolyte 12, see column 5, lines 55-57) and thin metal layer (15).

10. Claims 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki et al. (US. 6,084,796) in view of Gonzalez et al. (US. 6,391,688) as applied to claim 28 above, and further in view of Yadav et al. (US. 6,387,560).

With respected to dependent claim 31. Kozicki et al. in view of Gonzalez et al. disclose in a programming metallization cell memory above, for example, Kozicki et al in Figure 1A-1B and Figure 5C discloses a programming metallization cell memory (10) comprising: a pair of electrodes (13, 14 in Figure 1A-1B and 253, 254, 260, 262 in Figure 5C); a thin metal layer (metal 15, example, when the metal 15 which is apply the voltage for removed the electrodes 13 and 14, see column 6, lines 5-9); a single resistive layer (resistive 270, for example, 270 is a resistive material layer as shown in Figure 5C, see column 8, lines 50-58) with a plurality of solid electrolyte (ion conductor 12 in Figure 1A-1B including a solid electrolyte, see column 5, line 18-19); and Gonzalez et al in Figure 15 disclosed the ultra-small pore is the fabrication utilized of the chalcogenide memory cell (see column 6, lines 66-67 and column 7, lines 1-5).

However, Kozicki et al. in view of Gonzalez et al. does not disclose the size of the solid electrolyte range about 1-100nm (nanometer) in diameter.

Yadav et al. disclosed an ion conducting solid electrolytes which is grain size has been confined to dimensions less than 100 nanometers. (see column 6, lines 3-7).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the programming metallization cell memory of Kozicki et al in view of Gonzalez et al to include a size range of solid electrolytes base on ion defect structure as in Yadav et al for the purpose of easily and change the properties of the material.

### ***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

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Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see

<http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 6 2005